ECE 532H1 S – Digital Systems Design

Course Information

Winter 2021
Revision : 1.5 of February 16, 2021

1 Contacts

<table>
<thead>
<tr>
<th>Instructor</th>
<th>email</th>
<th>Office Hours</th>
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<tbody>
<tr>
<td>Paul Chow</td>
<td><a href="mailto:pc@eeecg.toronto.edu">pc@eeecg.toronto.edu</a></td>
<td>TBD</td>
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1.1 Discussion Board

We will use Piazza for the class discussion board. Piazza is now connected through Quercus. For information on joining the Piazza site for this course, please go to https://q.utoronto.ca/courses/46670/files/8508789/download?wrap=1.

Please post all of your course-related questions to Piazza as it is quite likely others will have the same question and it is good to have the responses available to everyone.

If you have a personal issue, please contact the instructors directly by email or a private Piazza post.

2 Required Text

No textbook.

3 Calendar Description

Fixed Credit Value: 0.50
Hours: 38.4L/38.4P

Advanced digital systems design concepts including project planning, design flows, embedded processors, hardware/software interfacing and interactions, software drivers, embedded operating systems, memory interfaces, system-level timing analysis, clocking and clock domains. A significant design project is undertaken and implemented on an FPGA development board.
4 Learning Outcomes

Leverage skills and knowledge gained so far, especially in the areas of hardware and software design, to design and implement a significant system-on-chip (SoC) on an FPGA board.

By working in typical groups of three students, develop the technical and management skills required to work as a team on a complex project.

By working as a team on a significantly complex system design, learn the processes required to achieve success that more closely reflects an industrial design environment.

Gain experience in designing a complete digital hardware system from initial concept to implementation and testing by implementing a significant design project on an FPGA board.

Learn how to incorporate processors into embedded systems and have the processors interact with hardware.

Learn fundamental concepts in embedded processor design and programming.

Learn fundamental concepts in clocking and dealing with multiple clock domains.

Learn techniques for high-speed interface design.

Learn about system-level timing analysis for high-speed interfaces.

Learn about FPGA design using modern CAD tools.

Learn about FPGA architectures and how to use advanced features of modern FPGAs.

5 Real-World Relevance

Computers are everywhere. This course covers some advanced topics of digital hardware design, which is the basis for designing all forms of computing.

6 Structure

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<th></th>
<th>Format</th>
<th>Number</th>
<th>Hours/week</th>
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<tbody>
<tr>
<td>Lectures</td>
<td>Synchronous*</td>
<td>3</td>
<td>3</td>
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<tr>
<td>Office Hours</td>
<td>Synchronous</td>
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<td>By appointment</td>
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<tr>
<td>Labs</td>
<td>Synchronous</td>
<td>11</td>
<td>3</td>
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* Some of the content will be delivered asynchronously reducing the number of synchronous lectures.

The course material will be presented both synchronously and asynchronously. Synchronous lectures will be for content that would benefit from more interaction from the class, but they will be
recorded for students unable to attend the live presentation. The goal for asynchronous content is to use short videos of 10-15 minutes with one video per topic that will be more suitable for online delivery.

Synchronous office hours are available by appointment.

The labs will be synchronous during 9am to 3pm on Wednesdays. The first three weeks are for doing tutorials to learn the tools and use the hardware. The remaining lab periods are for the design groups to meet with their TA manager. A TA will be available during the entire time.

There will be presentations required during the term and for the final project demo. These will be done synchronously, if possible, but could also be done by a video recording.

7 Timetable

Lectures

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<tr>
<th>L101</th>
<th>Synchronous Times</th>
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<tbody>
<tr>
<td></td>
<td>M 17:00-18:00</td>
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<td>W 17:00-18:00</td>
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<td>F 14:00-15:00</td>
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Labs

| TA Meetings | W 09:00–15:00 |

8 Grade Composition

Lab Demo 10%
Assignments 10%
Quiz 15%
Project 65%
Total 100%

9 Quiz Date

Quiz April 12, 2021
10 Assessment Scheme

Warmup Demo  This is a small exercise to demonstrate some basic competence in using the design tools and develop a small component that will be used in the projects.

Quiz  This a quiz held in a lecture period to test some of the lecture material.

Assignments  There are two assignments. One introduces the students to using some more advanced features of the FPGAs and tools. The second assignment introduces more advanced simulation techniques.

Project  This is the main component of the course. Each group of at least three students will implement a significant project on an FPGA board. This year, the project has been designed so that it can be implemented entirely in a remote setting. FPGA boards and PCs can all be accessed remotely.

Each group works with a managing TA who helps them to formulate the project and evaluates weekly milestones.

There is a final demonstration and two reports. One report is a group report about the overall project and one is an individual report where each student describes their own contribution and gives some reflections about the project.

11 Laboratory Experience

The first two labs provide training on using the tools through a number of hands-on tutorials. The remaining labs are open periods for students to work on their projects. Each group will meet with their managing TA once per week to discuss progress and current issues.

The projects require both hardware and software components and the students will gain experience on integrating software running on processors with their hardware.

This year, the project theme is FPGAs in the Cloud so students will also learn some basics about using networking for communication between FPGAs and CPUs and FPGAs with FPGAs.

12 Course Outline

There are two main goals of this course:

1. Gain digital system design experience by implementing a significant FPGA design.
2. Learn some advanced hardware design concepts during the lectures. These are generally not exercised during the projects.

12.1 Topics

- Design flow for large systems
- Mapping algorithms to architectures
- Performance estimation
- Memories
- Buses
- FPGA architecture and tools
- Simulation and verification
- Embedded programming
- Implementation technology spectrum
- Clocking
- Synchronizers
- High-speed interfaces, SERDES
- Introduction to high-level synthesis

13 Notice of video recording and sharing (Download permissible; re-use prohibited)

At times during this course, some interactions including your participation, may be recorded on video and will be available to students in the course for viewing remotely and after each session. Course videos and materials belong to the instructors, the University, and/or other source depending on the specific facts of each situation, and are protected by copyright. In this course, you are permitted to download session videos and materials for your own academic use, but you should not copy, share, or use them for any other purpose without the explicit permission of the instructor. For questions about recording and use of videos in which you appear please contact your instructor.
14 Academic Integrity Policies

http://www.academicintegrity.utoronto.ca/

For each midterm and the final assessment, you will be required to acknowledge and sign the following pledge:

I, _____________, pledge upon my honour that I will not violate our Faculty’s Code of Behaviour on Academic Matters during this assessment by acting in any way that would constitute cheating, misrepresentation, or unfairness, including but not limited to, using unauthorized aids and assistance, impersonating another person, and committing plagiarism. I acknowledge that providing unauthorized assistance to someone else is also considered a serious academic offence.

15 Land Acknowledgement

I (we) wish to acknowledge this land on which the University of Toronto operates. For thousands of years it has been the traditional land of the Huron-Wendat, the Seneca, and most recently, the Mississaugas of the Credit River. Today, this meeting place is still the home to many Indigenous people from across Turtle Island and we are grateful to have the opportunity to work on this land.

16 Inclusivity, Accommodations and Mental Health Support

16.1 Statement on Inclusivity

You belong here. The University of Toronto commits to all students, faculty and staff that you can learn, work and create in a welcoming, respectful and inclusive environment. In this class, we embrace the broadest range of people and encourage their diverse perspectives. This team environment is how we will innovate and improve our collective academic success. You can read the evidence for this approach here.

We expect each of us to take responsibility for the impact that our language, actions and interactions have on others. Engineering denounces discrimination, harassment and unwelcoming behaviour in all its forms. You have rights under the Ontario Human Rights Code. If you experience or witness any form of harassment or discrimination, including but not limited to, acts of racism, sexism, Islamophobia, anti-Semitism, homophobia, transphobia, ableism and ageism, please tell someone so we can intervene. Engineering takes these reports extremely seriously. You can talk to anyone you feel comfortable approaching, including your professor or TA, an academic advisor, our Assistant Dean, Diversity, Inclusion and Professionalism, the Engineering Equity Diversity and Inclusion Action Group, any staff member or a U of T Equity Office.
You are not alone. Here you can find a list of clubs and groups that support people who identify in many diverse ways. Working together, we can all achieve our full potential.

16.2 Statement on Accommodations

The University of Toronto supports accommodations for students with diverse learning needs, which may be associated with mental health conditions, learning disabilities, autism spectrum, ADHD, mobility impairments, functional/fine motor impairments, concussion or head injury, blindness and low vision, chronic health conditions, addictions, deafness and hearing loss, communication disorders and/or temporary disabilities, such as fractures and severe sprains, or recovery from an operation.

If you have a learning need requiring an accommodation the University of Toronto recommends that students register as soon as possible with Accessibility Services.
Phone: 416-978-8060
Email: accessibility.services@utoronto.ca

16.3 Statement on Mental Health

As a university student, you may experience a range of health and/or mental health challenges that could result in significant barriers to achieving your personal and academic goals. Please note, the University of Toronto and the Faculty of Applied Science & Engineering offer a wide range of free and confidential services that could assist you during these times.

As a U of T Engineering student, you have an Academic Advisor (undergraduate students) or a Graduate Administrator (graduate students) who can support you by advising on personal matters that impact your academics. Other resources that you may find helpful are listed on the U of T Engineering Mental Health & Wellness webpage, and a small selection are also included here:

- Accessibility Services & the On-Location Advisor
- Graduate Engineering Council of Students’ Mental Wellness Commission
- Health & Wellness and the On-Location Health & Wellness Engineering Counsellor
- Inclusion & Transition Advisor
- U of T Engineering Learning Strategist and Academic Success
- My Student Support Program (MySSP)
- Registrars Office
- SKULE Mental Wellness
- Scholarships & Financial Aid Office & Advisor
If you find yourself feeling distressed and in need of more immediate support resources, consider reaching out to the counsellors at My Student Support Program (MySSP) or visiting the Feeling Distressed webpage.