1 Contacts

<table>
<thead>
<tr>
<th>Instructor</th>
<th>email</th>
<th>Office Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Paul Chow, Course Coordinator</td>
<td><a href="mailto:pc@eecg.toronto.edu">pc@eecg.toronto.edu</a></td>
<td>TBD</td>
</tr>
<tr>
<td>Belinda Wang</td>
<td><a href="mailto:belinda.wang@utoronto.ca">belinda.wang@utoronto.ca</a></td>
<td>TBD</td>
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1.1 Discussion Board

We will use Piazza for the class discussion board. Piazza is now connected through Quercus. For information on joining the Piazza site for this course, please go to https://q.utoronto.ca/courses/46670/files/8508789/download?wrap=1. The same document is available as Piazza-Quercus Student Experience.pdf in Module 0.4.

Please post all of your course-related questions to Piazza as it is quite likely others will have the same question and it is good to have the responses available to everyone.

If you have a personal issue, please contact one of the instructors directly.

2 Required Text

Title: Fundamentals of Digital Logic with Verilog Design, 3rd Edition
Authors: Stephen Brown and Zvonko Vranesic
Publisher: McGraw-Hill
ISBN: 0073380547

3 Calendar Description

Fixed Credit Value: 0.50
Hours: 38.4L/38.4P

Digital logic circuit design with substantial hands-on laboratory work. Algebraic and truth table representation of logic functions and variables. Optimizations of combinational logic, using “don’t cares.” Multi-level logic optimization. Transistor-level design of logic gates; propagation delay
and timing of gates and circuits. The Verilog hardware description language. Memory in digital circuits, including latches, clocked flip-flops, and Static Random Access Memory. Set-up and hold times of sequential logic. Finite state machines - design and implementation. Binary number representation, hardware addition and multiplication. Tri-state gates, and multiplexers. There is a major lab component using Field-Programmable Gate Arrays (FPGAs) and associated computer-aided design software.

4 Learning Outcomes

Learn the types of logic gates, rules of Boolean Algebra and methods for minimizing logic expressions and then create logic expressions from word descriptions to determine and draw minimized logic circuits.

Learn about storage elements, such as latches, flip flops and memories, and then use them to create registers, counters, and memories in the labs.

Learn about finite state machines and how they are synthesized, and then use them to control datapaths as part of the lab exercises.

Learn about number representations, adders and multipliers and build arithmetic circuits as part of the lab exercises.

Given example working Verilog code and Verilog skeleton code, write Verilog circuit descriptions that are simulated using Modelsim and compiled and synthesized using Quartus for testing on an FPGA board.

From word descriptions of problems, create hardware designs that are implemented in Verilog and tested on an FPGA board.

Learn about logic delays and timing requirements for flip flops and determine the maximum frequency of operation for circuits.

Learn basic properties of MOS transistors, circuits for basic and complex gates and design simple transistor-level logic circuits.

5 Real-World Relevance

Computers are everywhere. This course covers the fundamentals of digital hardware design, which is the basis for designing all forms of computing.
6 Structure

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<th></th>
<th>Format</th>
<th>Number</th>
<th>Hours/week</th>
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<tbody>
<tr>
<td>Lectures</td>
<td>Asynchronous</td>
<td></td>
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<tr>
<td>Office Hours</td>
<td>Synchronous</td>
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<td>2 or 3, TBD</td>
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<tr>
<td>Labs</td>
<td>Synchronous</td>
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<td>3</td>
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The course material will be presented asynchronously using short videos, one video per topic. When you go to Quercus you will find a video in the Welcome module that will give you guidance on how to navigate the modules there.

Synchronous office hours will be scheduled. The schedule will be determined based on student input.

The labs are an important part of this course and is where most of your learning will take place. Becoming a good hardware designer cannot be done by reading books and doing problems. It comes with experience and requires mentorship to become really good. The apprenticeship model is probably the most appropriate to becoming a good hardware designer. If you ever look for a job in the area, also look for senior designers that can guide you.

The labs will be synchronous with a TA leading a group of about 15-16 students. Students will work individually. There is no need to pair up. There are a total of seven labs and, unfortunately, no project this year. The project requires lots of interactive team work, which is not possible at this time. We also feel that with the challenge of doing everything online, reducing the load will help to make the experience more manageable. More details on how labs will run will be provided as we figure it out. The first lab is currently scheduled for Monday, Oct. 5 so there is time to build a good plan for doing the labs.

7 Timetable

Lectures

| L101 | Asynchronous |

Labs

<table>
<thead>
<tr>
<th>P101</th>
<th>M 18:00–21:00</th>
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<tr>
<td>P102</td>
<td>M 15:00–18:00</td>
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<tr>
<td>P103</td>
<td>T 15:00–18:00</td>
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<td>P104</td>
<td>T 15:00–18:00</td>
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<tr>
<td>P105</td>
<td>M 09:00–12:00</td>
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<tr>
<td>P106</td>
<td>M 09:00–12:00</td>
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8 Grade Composition

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<tr>
<td>Labs</td>
<td>10%</td>
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<tr>
<td>Midterm 1</td>
<td>30%</td>
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<tr>
<td>Midterm 2</td>
<td>30%</td>
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<tr>
<td>Final</td>
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<td><strong>Total</strong></td>
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9 Midterm Dates

Midterm 1  October 15, 2020
Midterm 2  December 3, 2020 (rescheduled from November 26, 2020)

10 Assessment Scheme

**Labs**  There are seven (7) labs each worth 2%. The maximum grade for labs is 10% meaning you could miss two lab evaluations. To minimize the time for grading, TAs will only check that some work was attempted to achieve 2%. Reducing grading time will leave more time for helping the students. Note that about 25-30% of the midterms and final grades will be based on questions related to what you learn and do in the labs.

**Midterms and Final**  There are two components to these assessments. There will be a written component distributed and submitted using Crowdmark. There will also be an oral component via a video interview. If you want the option to request a re-evaluation of the oral component, you must agree to recording the interview with your camera turned on. The same setup will be used during the labs, so that is an opportunity for you test your equipment.

The current planned format for the tests is that you will have a limited time period to start and submit the test within a window of 24 hours.

**Mandatory Assessment**  The final exam (final summative assessment) is mandatory. If this mandatory component is not completed, the student will receive a grade of incomplete (INC).

11 Laboratory Experience

The first lab will start with the *logisim* gate-level to simulate basic logic circuits. The remaining labs will use the *Intel Quartus Prime* tools for FPGA design using Verilog. Quartus is a commercial tool used for FPGA design. In this environment where we cannot access real hardware, it is not
really necessary to use Quartus to validate your code. We will still require you to use Quartus so that you gain that experience for use in future courses or possibly in jobs you get in the future.

Unfortunately, without access to the physical labs your designs will have to be tested via simulation. To provide an experience as close as possible to interacting with the real hardware, we have developed a GUI to provide the equivalent switches, buttons, LEDs and 7-segment displays as are on the real board so that you can interact with your designs as if they are running on the real hardware. The main difference is that the circuit will not run as fast as it would in the real hardware.

12 Course Outline

There are three main goals of this course:

1. To understand basic digital logic circuit design, optimization and concepts.
2. To become comfortable using Computer-Aided Design (CAD) tools in design.
3. To gain hands-on experience with the design and debug of digital systems, using programmable logic.

12.1 Introduction to Combinational Logic

- switches and logic gates
- logic functions, truth tables and variables
- Boolean axioms and laws, sum of products, product of sums
- simple algebraic minimization - making things cheaper with a new kind of algebra

12.2 Technology

- logic voltage levels
- transistors as a switch
- NMOS and CMOS logic gates
- real propagation delay, and timing diagrams, timing analysis of digital circuits
- Field-Programmable Gate Arrays (FPGAs)
- introduction to Verilog (a language for describing hardware) and CAD tools that implement hardware given the Verilog description language
12.3 Combinational Logic Optimization

- minimization goals - speed and cost
- Karnaugh Map optimization technique
- optimization of logic that have Don’t Care conditions
- critical path through combinational logic

12.4 Sequential Logic

- cross-coupled NOR/NAND gates basic latch
- gated latch
- Master-Slave D flip-flop
- shift registers
- counters
- set-up and hold time, clock-to-Q

12.5 Finite State Machines

- how logic is controlled
- state diagrams
- Moore-type state machines, Mealy-type machines
- state machine synthesis
- state machines in Verilog
- state encoding and optimization

12.6 Numbers and Arithmetic

- number representation, binary, ones and twos complement representation of negative numbers
- basic adder/subtractor
- carry look-ahead methods for fast addition
- bit serial addition
12.7 Miscellaneous

- multiplexors and tristate gates
- multiplexors as logic; decoders, encoders
- fanout-dependent delay
- power dissipation, I/O devices and FPGAs
- Static Random Access Memory (SRAM);
- controller for digital display
- de-bouncing mechanical switches
- VGA display interface

13 Notice of video recording and sharing (Download permissible; re-use prohibited)

At times during this course, some interactions including your participation, may be recorded on video and will be available to students in the course for viewing remotely and after each session.

Course videos and materials belong to the instructors, the University, and/or other source depending on the specific facts of each situation, and are protected by copyright. In this course, you are permitted to download session videos and materials for your own academic use, but you should not copy, share, or use them for any other purpose without the explicit permission of the instructor. For questions about recording and use of videos in which you appear please contact your instructor.

14 Academic Integrity Policies

http://www.academicintegrity.utoronto.ca/

For each midterm and the final assessment, you will be required to acknowledge and sign the following pledge:

I,______________, pledge upon my honour that I will not violate our Faculty’s Code of Behaviour on Academic Matters during this assessment by acting in any way that would constitute cheating, misrepresentation, or unfairness, including but not limited to, using unauthorized aids and assistance, impersonating another person, and committing plagiarism. I acknowledge that providing unauthorized assistance to someone else is also considered a serious academic offence.
15 Land Acknowledgement

I (we) wish to acknowledge this land on which the University of Toronto operates. For thousands of years it has been the traditional land of the Huron-Wendat, the Seneca, and most recently, the Mississaugas of the Credit River. Today, this meeting place is still the home to many Indigenous people from across Turtle Island and we are grateful to have the opportunity to work on this land.

16 Inclusivity, Accommodations and Mental Health Support

16.1 Statement on Inclusivity

You belong here. The University of Toronto commits to all students, faculty and staff that you can learn, work and create in a welcoming, respectful and inclusive environment. In this class, we embrace the broadest range of people and encourage their diverse perspectives. This team environment is how we will innovate and improve our collective academic success. You can read the evidence for this approach here.

We expect each of us to take responsibility for the impact that our language, actions and interactions have on others. Engineering denounces discrimination, harassment and unwelcoming behaviour in all its forms. You have rights under the Ontario Human Rights Code. If you experience or witness any form of harassment or discrimination, including but not limited to, acts of racism, sexism, Islamophobia, anti-Semitism, homophobia, transphobia, ableism and ageism, please tell someone so we can intervene. Engineering takes these reports extremely seriously. You can talk to anyone you feel comfortable approaching, including your professor or TA, an academic advisor, our Assistant Dean, Diversity, Inclusion and Professionalism, the Engineering Equity Diversity and Inclusion Action Group, any staff member or a U of T Equity Office.

You are not alone. Here you can find a list of clubs and groups that support people who identify in many diverse ways. Working together, we can all achieve our full potential.

16.2 Statement on Accommodations

The University of Toronto supports accommodations for students with diverse learning needs, which may be associated with mental health conditions, learning disabilities, autism spectrum, ADHD, mobility impairments, functional/fine motor impairments, concussion or head injury, blindness and low vision, chronic health conditions, addictions, deafness and hearing loss, communication disorders and/or temporary disabilities, such as fractures and severe sprains, or recovery from an operation.

If you have a learning need requiring an accommodation the University of Toronto recommends that students register as soon as possible with Accessibility Services.
Phone: 416-978-8060
Email: accessibility.services@utoronto.ca
16.3 Statement on Mental Health

As a university student, you may experience a range of health and/or mental health challenges that could result in significant barriers to achieving your personal and academic goals. Please note, the University of Toronto and the Faculty of Applied Science & Engineering offer a wide range of free and confidential services that could assist you during these times.

As a U of T Engineering student, you have an Academic Advisor (undergraduate students) or a Graduate Administrator (graduate students) who can support you by advising on personal matters that impact your academics. Other resources that you may find helpful are listed on the U of T Engineering Mental Health & Wellness webpage, and a small selection are also included here:

- Accessibility Services & the On-Location Advisor
- Graduate Engineering Council of Students’ Mental Wellness Commission
- Health & Wellness and the On-Location Health & Wellness Engineering Counsellor
- Inclusion & Transition Advisor
- U of T Engineering Learning Strategist and Academic Success
- My Student Support Program (MySSP)
- Registrars Office
- SKULE Mental Wellness
- Scholarships & Financial Aid Office & Advisor

If you find yourself feeling distressed and in need of more immediate support resources, consider reaching out to the counsellors at My Student Support Program (MySSP) or visiting the Feeling Distressed webpage.