Course Content:

1. VLSI Technology
   A historical perspective, evolution of technology and market status. Silicon wafer manufacturing, wafer cleaning, oxidation, diffusion/drive-in, ion-implantation, CVD/epitaxy, metallization, photolithography, mask making, wet/dry etching, wafer probing, dicing, packaging, process and device simulation

2. Small-Geometry MOSFETs for VLSI
   Review of the MOSFET structure and operation. Threshold Voltage Corrections for Small MOSFETs, Short Channel, Narrow Width, and Minimum Size Effects, Two-dimensional MOSFET Effects, Subthreshold Operation, MOSFET Scaling Limitations, FINFETs

3. SPICE MOSFET Models
   Level 1, 2, and 3 Models, BSIM Model, other compact models. Spice Model Parameter Extraction

4. Bipolar Junction Transistors
   BJT structures and operation, Gummel-Poon and HiCUM models, Breakdown Voltage and Frequency Limitations, Small Signal Equivalent Circuits and Cutoff Frequencies, High Current Effects and Transient Behaviors

5. Process Integration
   Overview of the CMOS technology: single well, twin well, LOCOS and shallow trench isolation, Bipolar and BiCMOS processes, RF BiCMOS, SOI-CMOS, HVCMOS, DRAM, flash memory, embedded memory

6. Integrated Circuit Design
   Layout design rules, isolation, latch-up and matching considerations, MOSFET, BJT, resistor, capacitor, inductor layouts, test patterns, process control modules, component sizing, line width and alignment issues, VLSI chip layout, standard cells, power ground considerations

7. Design Flow
   Overview of VLSI design methodology, floor planning, design specifications, schematic entry, netlist generation, levels of simulation, handcrafted layout, synthesized layout, layout extraction, DRC, ERC, LVS, post layout simulation, tape-out.

8. Special Purpose Semiconductor Devices
   GaN HEMTs, graphene devices, carbon nano-tube devices, power devices, heterojunctions, InP and GaSb HBTs, EEPROMs
Labs/Design Project:

Lab #1  N-Well Resistor Process and Device Simulation

CAD (Computer Aided Design) is an import tool for the development of integrated circuit fabrication processes and semiconductor devices. In this laboratory, the basic simulation procedures will be introduced via the virtual construction and testing of an n-well resistor.

TSUPREM4 and MEDICI are a pair of popular CAD programs used to simulate the fabrication and electrical characteristics of semiconductor devices. A typical simulation cycle starts with the fabrication of the semiconductor devices using TSUPREM4. The process starts with the creation of a geometric model of the semiconductor material. The output information provided by the program includes structure geometry, doping profiles and mechanical stress induced by oxidation, thermal cycling, or film deposition. The program also allows the user to examine the device along different regions. After the semiconductor device is produced by TSUPREM4, structure information is passed onto MEDICI, which can analyze the response from applied voltages or currents.

Lab #2  MOSFET and BJT Process and Device Simulation

In the previous lab assignment, two-dimensional TCAD simulators TSUPREM4 and MEDICI were introduced to simulate the fabrication and electrical characteristics of an n-well resistor. In this laboratory, a simplified CMOS/BiCMOS process and the electrical characteristics of the devices will be simulated.

This lab is divided into two parts, with the first section covering the simulation of a MOSFET and the second section covering the simulation of a BJT, all in a 0.18μm BiCMOS process.

Lab #3  Schematic Entry and Layout in Cadence (90 nm CMOS)

In lab #2 students learned to manipulate a mask file in order to generate a desired single-transistor structure. Cadence Virtuoso is a layout tool that makes it easy to manipulate masks in order to generate complex transistor patterns on a single chip. In TSUPREM students generated 2-dimensional cross-sections of various devices. In Cadence, students will instead be generating top views of these devices by defining the appropriate mask areas.

Lab #4  CMOS Diff Pair Circuit Simulation and Layout (90-nm CMOS)

In the previous lab students learned to create a schematic and layout of a single NMOS transistor. In this lab students will expand upon this design by adding both NMOS and PMOS devices in order to create a CMOS differential pair. Students will need to reuse many commands from previous lab.

In this lab students will learn how to detrimental the effects of mismatch and process variations on the performance of a simple CMOS differential pair. Students will experiment with different layout techniques that will help minimize these effects.

Lab #5  Integrated Op Amp Design (90-nm CMOS)

Student will be given a complete design exercise for an op amp circuit from schematic simulation, layout, to post layout simulation. Students will learn how the circuit layout, power budget and fabrication technology affect the overall performance of the CMOS op amp.