ECE 241F – Digital Systems

Fall 2014 – P. Chow, B. Wang

Basic Information

Instructors and Lecture Information

<table>
<thead>
<tr>
<th>Section</th>
<th>1</th>
<th>2</th>
<th>3</th>
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</thead>
<tbody>
<tr>
<td>Instructor</td>
<td>Paul Chow</td>
<td>Belinda Wang</td>
<td>Belinda Wang</td>
</tr>
<tr>
<td>Office</td>
<td>EA 320</td>
<td>GB 250</td>
<td>GB 250</td>
</tr>
<tr>
<td>Phone</td>
<td>416-978-2402</td>
<td>416-978-5543</td>
<td>416-978-5543</td>
</tr>
<tr>
<td>Email</td>
<td><a href="mailto:pc@eecg.toronto.edu">pc@eecg.toronto.edu</a></td>
<td><a href="mailto:belinda.wang@utoronto.ca">belinda.wang@utoronto.ca</a></td>
<td><a href="mailto:belinda.wang@utoronto.ca">belinda.wang@utoronto.ca</a></td>
</tr>
<tr>
<td>Office hours</td>
<td>Arrange with your instructor by email</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lecture Rooms/Times</td>
<td>M 5-6 SF 1101 M 4-5 BA 1170 M 11-12 BA 1180</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>W 5-6 SF 1101 T 5-6 SF 1101 W 11-12 BA 1180</td>
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<td>R 5-6 SF 1101 R 4-5 SF 1101 R 11-12 BA 1180</td>
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Informal Tutorial
There will be 8 informal tutorials held starting Thursday, Sept. 18 through to Thursday, Nov. 6. These tutorials will give some guidance on the lab preparation for the following week. The goal is to have two sessions: 1-2 and 2-3. One will also be recorded and made available online. More details coming.

Grading

| Labs 10% | Project 10% | Midterm 30% | Exam 50% |

Web Page:
Blackboard Portal – mainly for grades, secure stuff
www.piazza.com – discussion board, handouts – see Blackboard announcement for more details

Midterm
Thursday, October 16, 2014 6-8 PM. Put it in your calendar!

Exam
Type D – examiner specified aids: One single sheet of letter size paper (8.5x11 inch) with your written notes of your own choosing. No calculators, no cell phones.

Required Text
Title: Fundamentals of Digital Logic with Verilog Design, 3rd Edition
Authors: Stephen Brown and Zvonko Vranesic
Publisher: McGraw-Hill
ISBN: 0073380547

Running CAD Software at Home
See the syllabus page on CAD software to find out how to obtain the software for your computer and what kind of computer is required.
ECE 241F - Digital Systems - Course Outline

Goals

1. To understand basic digital logic circuit design, optimization and concepts.
2. To become comfortable using Computer-Aided Design (CAD) tools in design.
3. To gain hands-on experience with the design and debug of digital systems, using programmable logic.

1. Introduction to Combinational Logic
   - switches and logic gates
   - logic functions, truth tables and variables
   - Boolean axioms and laws, sum of products, product of sums
   - simple algebraic minimization - making things cheaper with a new kind of algebra

2. Technology
   - logic voltage levels
   - transistors as a switch
   - NMOS and CMOS logic gates
   - real propagation delay, and timing diagrams, timing analysis of digital circuits
   - Field-Programmable Gate Arrays (FPGAs)
   - introduction to Verilog (a language for describing hardware) and CAD tools that implement hardware given the Verilog description language

3. Combinational Logic Optimization
   - minimization goals - speed and cost
   - Karnaugh Map optimization technique
   - optimization of logic that have “Don't Care” conditions
   - critical path through combinational logic
4. **Sequential Logic**

- cross-coupled NOR/NAND gates basic latch
- gated latch
- Master-Slave D flip-flop
- shift registers
- counters
- set-up & hold time, clock-to-Q

5. **Finite State Machines**

- how logic is controlled
- state diagrams
- Moore-type state machines, Mealy-type machines
- state machine synthesis
- state machines in Verilog
- state encoding and optimization

6. **Numbers and Arithmetic**

- number representation, binary, ones & twos complement representation of negative numbers
- basic adder/subtractor
- carry look-ahead methods for fast addition
- bit serial addition

7. **Miscellaneous**

- multiplexors & tristate gates
- multiplexors as logic; decoders
- fanout-dependent delay
- power dissipation, I/O devices and FPGAs
- Static Random Access Memory (SRAM);
- controller for digital display
- de-bouncing mechanical switches
- VGA display interface
The real learning in this course goes on in the laboratory where you design, build and test and fix real circuits. There are seven mandatory labs of three hours each, and so you will have one 3-hour lab every week. You will work in groups of two.

There is also a project based on the material of this course that you will also work with your partner on.

There are two parts to the lab experience: preparation, which you must do outside of the lab hours, and the actual implementation of circuits in the lab.

**Preparation**

Each lab usually requires you to do a significant amount of preparation, and is where you must do much of the work to understand the concepts. Preparation must be complete before the lab begins. Preparation will usually require design using the CAD software supplied. Each partner in the group of 2 must perform and submit a separate preparation. While it is acceptable to discuss your preparation with your partner, your work may not be copied from your partner; you will be required to explain your preparation. Please be aware that severe penalties will be imposed for copying of labs, as evidenced by an inability to explain the work given as preparation. It will be graded by the TAs at the beginning of the lab, on the following basis:

<table>
<thead>
<tr>
<th>Judgement of TA</th>
<th>Grade</th>
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<tbody>
<tr>
<td>Unable to explain any part of preparation</td>
<td>0</td>
</tr>
<tr>
<td>Some merit to work</td>
<td>1</td>
</tr>
<tr>
<td>Made a legitimate attempt</td>
<td>2</td>
</tr>
<tr>
<td>Reasonable job, may be some missing things</td>
<td>3-4</td>
</tr>
<tr>
<td>Correct and done well, demonstrated clear knowledge of subject.</td>
<td>5</td>
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**In-Lab Work**

In each lab you will typically have to build a working circuit. Once this is done, for each such circuit, show it to your TA for grading, out of 3:

<table>
<thead>
<tr>
<th>Judgement of TA</th>
<th>Grade</th>
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<tbody>
<tr>
<td>Did not attend or try</td>
<td>0</td>
</tr>
<tr>
<td>Tried, but failed to get much working</td>
<td>1</td>
</tr>
<tr>
<td>Most, but not all working</td>
<td>2</td>
</tr>
<tr>
<td>Everything worked</td>
<td>3</td>
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</table>

Note: Although the lab portion of the course is worth only 10%, both the midterm and the final exam will contain questions directly related to skills learned in the lab.
Lab Workstation Number and Maintenance
Each digital workstation that you’ll be sitting at has a number. Please use the same station each week. If a piece of equipment is not working, please tell a TA to tag the board with the problem and notify someone to have it repaired. Otherwise it will be broken the next time you need to use it!

Lab Sections, Day Time and Location

<table>
<thead>
<tr>
<th>Section</th>
<th>Day</th>
<th>Time</th>
<th>Location(s)</th>
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<tbody>
<tr>
<td>1,2</td>
<td>Friday</td>
<td>9am-12</td>
<td>BA 3135, 3145, 3155</td>
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<tr>
<td>3,4</td>
<td>Monday</td>
<td>9am-12</td>
<td>BA 3135, 3145, 3155</td>
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<tr>
<td>5,6</td>
<td>Friday</td>
<td>3pm-6pm</td>
<td>BA 3135, 3145, 3155</td>
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Lab and Project Schedule for 2014

<table>
<thead>
<tr>
<th>Date of Monday</th>
<th>Lab</th>
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<tbody>
<tr>
<td>September 8</td>
<td>No lab.</td>
</tr>
<tr>
<td>September 15</td>
<td>#1: Building simple logic functions using 7400-series chips.</td>
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<tr>
<td>September 22</td>
<td>#2 Lights, switches, multiplexers (before this lab, you should do the self-guided Quartus tutorial on your own).</td>
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<tr>
<td>September 29</td>
<td>#3 Numbers and displays</td>
</tr>
<tr>
<td>October 6</td>
<td>#4 Latches, flip-flops and registers</td>
</tr>
<tr>
<td>October 13</td>
<td>Thanksgiving week – no lab; midterm exam this week!</td>
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<tr>
<td>October 20</td>
<td>#5 Counters and clocks, arithmetic</td>
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<tr>
<td>October 27</td>
<td>#6 Finite state machines (FSMs)</td>
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<tr>
<td>November 3</td>
<td>#7 FSMs, VGA</td>
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<tr>
<td>November 10</td>
<td>Project Period 1</td>
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<tr>
<td>November 17</td>
<td>Project Period 2</td>
</tr>
<tr>
<td>November 24</td>
<td>Project Period 3</td>
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The lab in this course depends heavily on the use of Computer-Aided Design (CAD) software to implement the circuits, usually on a programmable logic device. We will be using Field-Programmable Gate Arrays (FPGAs) from Altera, and Altera’s Quartus II Version 11.1 CAD software. You will be able to access this software in one of three ways:

1. **On your own home computer.**

   If you have a Windows 7, Vista, XP or Linux-based home computer with at least 1 GBytes of physical RAM, you can download the Quartus II 11.1 SP2 Web edition directly from the Altera web site:


   In the lab we will be using the full version of the software, but the web edition has all you need as well.

   If you do not have this class of computer, you will be able to use the University’s machines instead.

2. **On the Windows Machines in the lab – Bahen 3135, 3145, 3155, 3165**

   There are a total of one hundred Windows 7-based machines in these Bahen Centre labs. These will have the latest release of the full license (not the web edition) of Quartus version 11.1 SP2 software installed on them. These machines will have access to your home directory on the ECE network.
ECE 241 Project

The Task

The purpose of the project is to:

1. Gain experience dealing with the design of a larger digital system, and to deal with the issues in going from a soft simple specification (“make a digital toaster controller”) to an actual complete design. There is no substitute for experience!

2. Express your creativity by applying what you have learned in this course to a project of your own choosing.

You will design and implement a project of your own choosing that uses digital logic in some creative way. You may use any of the parts available in the lab, but are restricted to using just one of the Altera DE2 boards. An important part of this lab is the creativity required to think up an interesting project, and then negotiate with a TA or instructor as to the final form of the project.

Originality/Uniqueness Approval

The first step in your project is to come up with an original idea. You must submit your idea, in a 1-3 line description, via email to the ECE241 head TA (email address TBA) for “originality” or “uniqueness” approval (you may also CC your instructor). The head TA will quickly respond to tell you if the idea has already been proposed more than once. If it has, you'll have to come up with something different. Please note that this approval is only the first step and only deals with the basic idea, and not the scope/effort required for the project; that comes next:

Before the First Project lab

You will submit a short project proposal of what your project is about. This should be a short description that gives:

- The basic idea of the project, and the basic function of your circuit.
- Describe the inputs and outputs, and give a simple block diagrams describing how the various parts of your circuit interact.
- Your plan of action for each of the three lab periods - "milestones"
- Present this to your TA to get their opinion on whether the project is viable. Once approved, you should get their signature. This is just a check to make sure that you do not try something overly ambitious.

Demonstration and Report

You will demonstrate your project to your supervising TA in the final lab period, and will be required to provide a short report describing your project.