Seeking Opportunities for Hardware Acceleration in Big Data Analytics

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Who am I?

I am interested in building computing machines/accelerators

Why accelerate?

To go faster, to reduce power

How to accelerate?

We use FPGAs

What are we doing?

Some of our projects

What are the opportunities in Big Data?
Moore’s Law

Microprocessor Transistor Counts 1971-2011 & Moore’s Law

- The graph illustrates the trend of transistor counts in microprocessors from 1971 to 2011.
- The line shows that the transistor count doubles every two years, aligning with Moore’s Law.
- This pattern is evident from the introduction of Intel’s Pentium processors to the latest Intel processors.

Date of introduction vs. Transistor count.
Until...

I’m melting!!!!
- Wizard of Oz 1939
More cores!!!

Programming hard and it’s not always fast enough
Need for accelerators

GPUs

FPGAs
What about these FPGAs?

First, a quick introduction....
FIELD-PROGRAMMABLE GATE ARRAYS
FIELD-PROGRAMMABLE GATE ARRAYS

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Hardwired FPGA functions

ARM A9
ARM A9

SRAM
Ser Des

DSP

1GE MAC
Computing with FPGAs

- Fully customized dataflow and buffering
- Tightly coupled pipelining of computations
- Very low energy / computation ratio
Example: Smith-Waterman DNA sequencing (Dynamic Programming)

49x – 980x speedup (I/O dependent) on Xilinx V4-LX160 FPGA vs. 2.2GHz AMD Opteron

(Storaasli/Cray 2009)
Molecular Dynamics

• Simulate motion of molecules at atomic level
• Highly compute-intensive
• Understand protein folding
• Computer-aided drug design
Platform for MD

- 12 short range nonbond FPGAs
- 2-3 pipelines/NBE FPGA; Each runs 15-30x CPU
- NBE 360-1080x

- 2 PME FPGAs with fast memory and fibre optic interconnects
- PME 420x

- Bonds on quad-core Xeon server
- Bonds 1x

Initial Breakdown of CPU Time

Sys Mem

Quad Xeon

Socket 1

8.5 GB/s @ 1066 MHz

Tools to Tackle Big Data
Performance

• Significant overlap between all force calculations.
• 108.02 ms is equivalent to between 80 and 88 Infiniband-connected cores at U of T’s supercomputer, SciNet.
• 160-176 hyperthreaded cores
• Can we do better?
  – 140 with hardware bond engines – change engine from SW to HW, no architectural change

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Tools to Tackle Big Data
More Recently

ISCA 2014   June 16, 2014

A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services

• Demonstrates that FPGAs can work in a data centre
• Accelerate the Bing ranking engine
• Double performance for only 10% increase in power
• To be deployed in Bing in 2015!
Traditional Programming of an FPGA
Design Flow

Figure 12.1. A typical CAD system.

Placement

Figure 12.8. Placement of the circuit in Figure 12.6.

Routing

Figure 12.9. Routing for the placement in Figure 12.8.

## Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Actual</th>
<th>Required</th>
<th>Slack</th>
<th>From</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{max}$</td>
<td>261.1 MHz</td>
<td>200 MHz</td>
<td>1.17 ns</td>
<td>AddSub</td>
<td>Overflow</td>
</tr>
<tr>
<td>$t_{su}$</td>
<td>2.356 ns</td>
<td>10.0 ns</td>
<td>7.644 ns</td>
<td>$b_0$</td>
<td>$breg_0$</td>
</tr>
<tr>
<td>$t_{co}$</td>
<td>6.772 ns</td>
<td>10.0 ns</td>
<td>3.228 ns</td>
<td>$xreg_0$</td>
<td>$z_0$</td>
</tr>
<tr>
<td>$t_h$</td>
<td>0.240 ns</td>
<td>10.0 ns</td>
<td>9.76 ns</td>
<td>$b_1$</td>
<td>$breg_1$</td>
</tr>
</tbody>
</table>

Table 12.1. A summary of static timing analysis results.

FPGA Programmability Drawbacks

• Need to understand hardware design
• Implementation (compile-equivalent) takes hours
• Established Hardware Description Languages (Verilog HDL, VHDL) are very low-level
• Downside of design flexibility:
  No established programming models
Programmability is Improving

• Higher-level HDLs
  – SystemC, SystemVerilog, Bluespec

• High-Level-Synthesis ("C-to-gates")
  – Very active area in research and industry, but:
  – So far, only useful if programmer understands hardware
  – Target not just an instruction set
    • designing the processor too!
  – Higher level of abstraction allows easier design exploration
    • Today, possible to achieve better than hand design in some cases
So, why are FPGAs still interesting?

- Even at 10% of a CPU/GPU clock rate
- Very high performance for the right applications
  - Building an application-specific computer
  - Custom memory architectures
  - Data stream processing especially fits
    - Caches don’t get in the way
  - Fine-grain parallelism
  - Bit manipulation
  - Pattern matching
- Performance per watt
  - 25W per chip versus 150W per chip
- Compute density
  - Racks of servers reduced to less than one
Often used closer to the data
SOME POSSIBLY RELEVANT PROJECTS
FPGAs as OpenStack Cloud Resources

Now we can “boot” a network connected FPGA accelerator on demand, in seconds!

- Framework for HLS – use HLS to create and then “drop in” accelerators
Example

- Dynamically scalable according to demand
- Same OpenStack command to boot/release either resource!

Site Requests

Uploads

VM Resource

Web Server

VFR

Data analysis engine

x10 000

Data Center

Outside World

Internal Network
Accelerators under Hadoop

- A Hadoop cluster with one x86 as master node and eight ZedBoards as slave nodes
  - FPGA: computation
  - ARM processor: communication and task tracing
MapReduce Data Flow

Map

Reduce

Result

Data0 → Map → Reduce → Result

Data1 → Map

Data2 → Map

HDFS

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Tools to Tackle Big Data
MapReduce Data Flow
MapReduce Data Flow with FPGA

HDFS → FPGA → FPGA → FPGA

Reduce

HDFS

July 3, 2014 Tools to Tackle Big Data
PGAS: Global Shared Memory

- Easy data transfers between all system memories
- Productive but efficient high-level programming model

Host CPU (x86)
- DRAM
  - Application
  - Soft API
  - Network Drivers

DRAM

Network

FPGA
- SRAM
  - Embedded CPU
    - Application
    - Soft API
  - Hard API

- SRAM
  - Custom Hardware
  - Hard API
HPC system: BEE4 + PC hosts

PCIe 2 x8 3.2 GB/s

2x 16GB DDR3-800

1Gb Eth

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Tools to Tackle Big Data
Low power, embedded system: Zynq

[Diagram of Zynq architecture with labels for DRAM, BlockRAM, Gc, CH, and 1 Gbit Ethernet]

x8
Big Data Memory Systems

To explore the use of FPGAs in the architecture of Big Data memory systems
Are there better memory architectures?

Replace middleware in-memory system with application-specific architecture
We Need Applications!

• We are not users
• We do not understand the applications
• Do you have a potential application?
• We could collaborate …

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Conclusions

- FPGAs are handicapped by the tools – hard to use
  - Good – Abstraction is being raised
  - Bad – Iteration time is very long – can be hours
- FPGAs can provide better performance for many interesting applications
- FPGAs can provide better performance per watt
- There should be good opportunities for FPGAs in Big Data – what are they?
Thank you for your attention!

Questions?

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